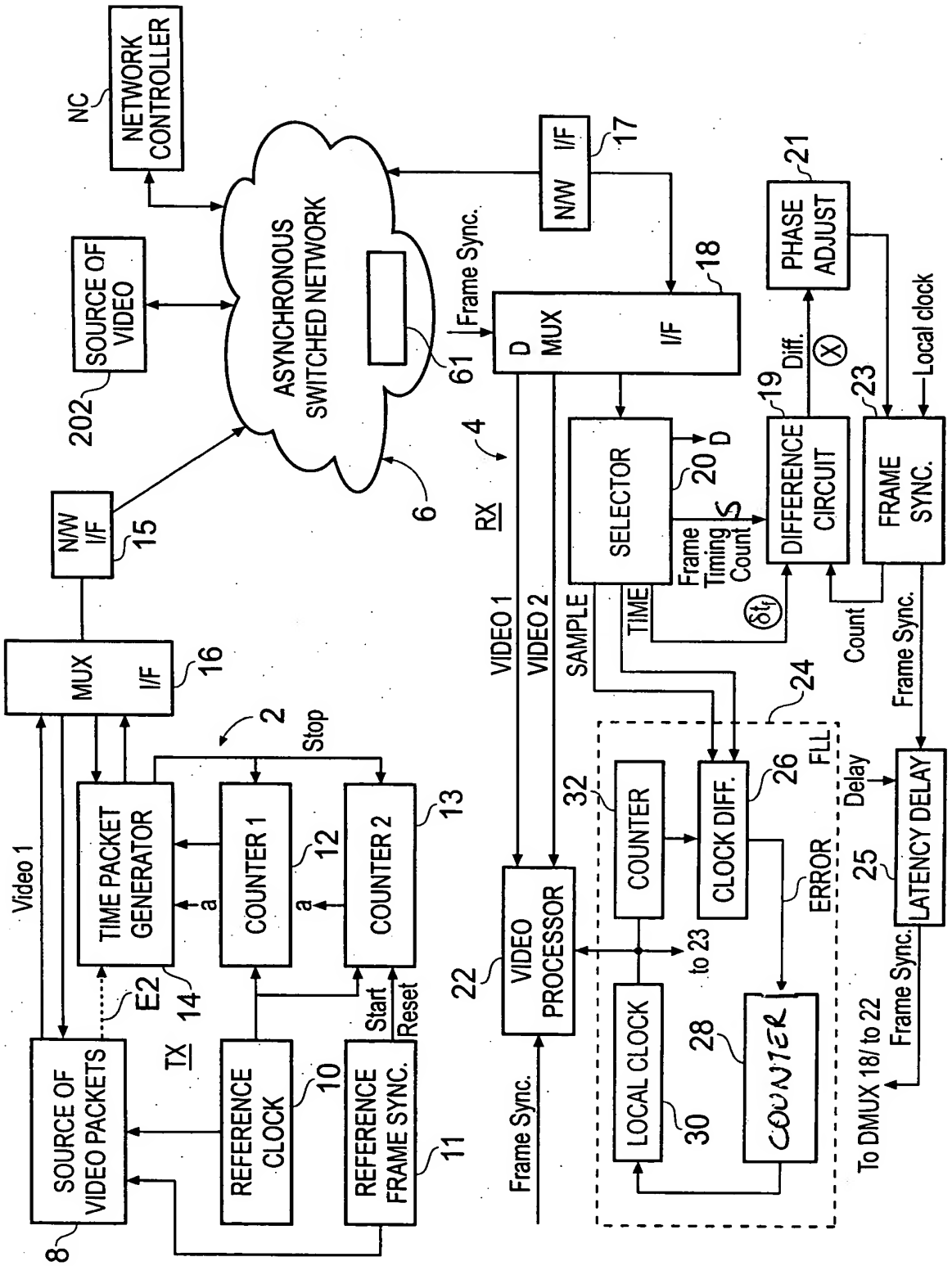
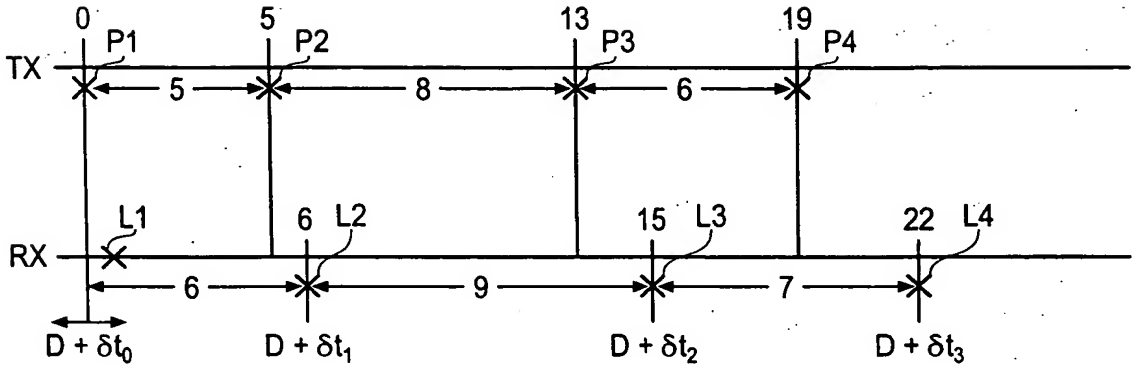

NC
NETWORK CONTROLLER
SOURCE OF VIDEO
202
ASYNCHRONOUS SWITCHED NETWORK
6
61
N/W I/F
15
N/W I/F
17
Frame Sync.
D MUX
I/F
18
PHASE ADJUST
21
RX
4
SELECTOR
20
D
Frame Timing Count
S
DIFFERENCE CIRCUIT
19
Diff.
X
FRAME SYNC.
23
Local clock
MUX
I/F
16
2
Stop
Video 1
TIME PACKET GENERATOR
a
COUNTER 1
12
a
COUNTER 2
13
VIDEO 1
VIDEO 2
SAMPLE
TIME
Count
Frame Sync.
24
E2
14
TX
SOURCE OF VIDEO PACKETS
8
REFERENCE CLOCK
10
Start
Reset
REFERENCE FRAME SYNC.
11
VIDEO PROCESSOR
22
32
COUNTER
CLOCK DIFF.
26
FLL
Delay
ERROR
25
LATENCY DELAY
Frame Sync.
to 23
LOCAL CLOCK
30
28
COUNTER
To DMUX 18/ to 22
Frame Sync.

Fig. 1



Second, RX, diff.	6	9	7
First, TX, diff.	5	8	6
Error	1	1	1
Cumulative Error	1	2	3

Fig. 2

Ethernet Frame Header	IP Datagram Header	UDP Header	Time stamp Data	Frame Timing Data	CRC

Fig. 3: UDP Timing Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Video Data	CRC

Fig. 7: Video Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Timestamp Data	Frame Timing Data	Video Data	CRC

Fig. 8: Combined Packet

Ethernet Frame Header	IP Datagram Header	UDP Header	Frame Timing Data	CRC

Fig. 9: UDP Frame Timing Packet

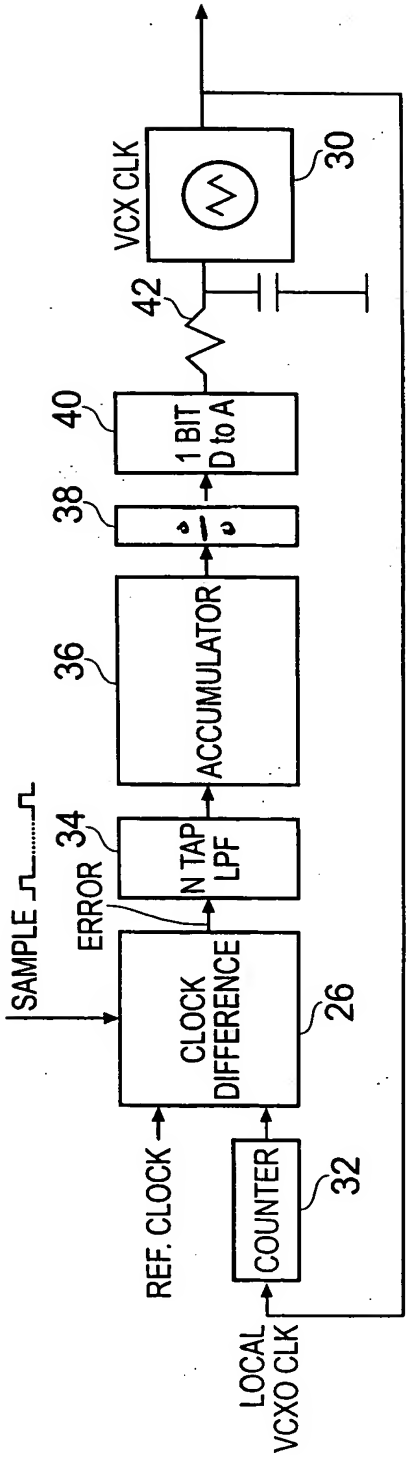


Fig. 4: Frequency Locking System

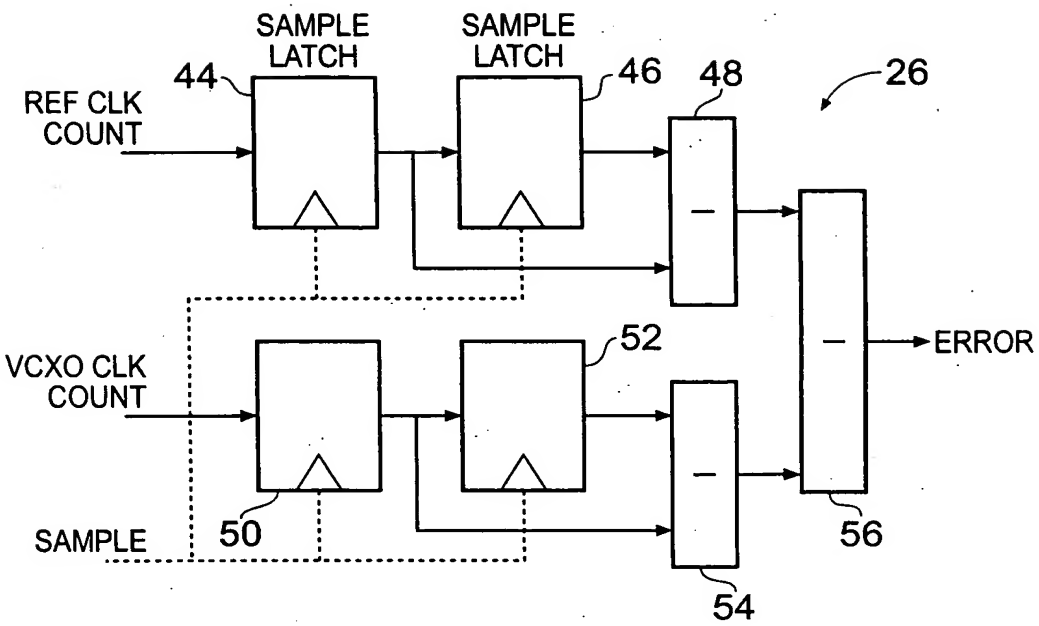


Fig. 5: Clock Difference Circuit

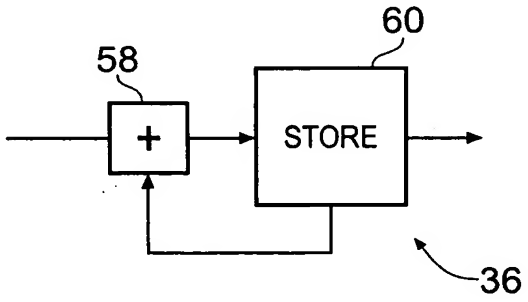


Fig. 6: Accumulator

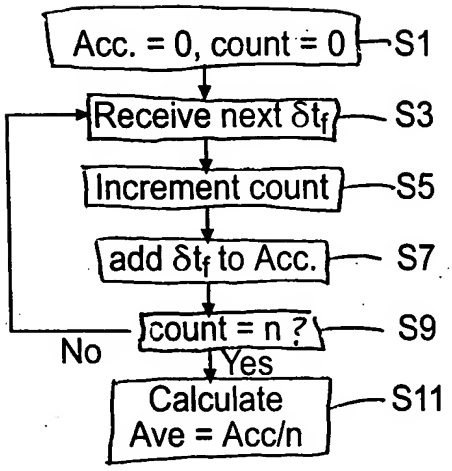

Acc. = 0, count = 0
S1
Receive next δt_f
S3
Increment count
S5
add δt_f to Acc.
S7
count = n ?
S9
No
Yes
Calculate
Ave = Acc/n
S11

Fig. 11

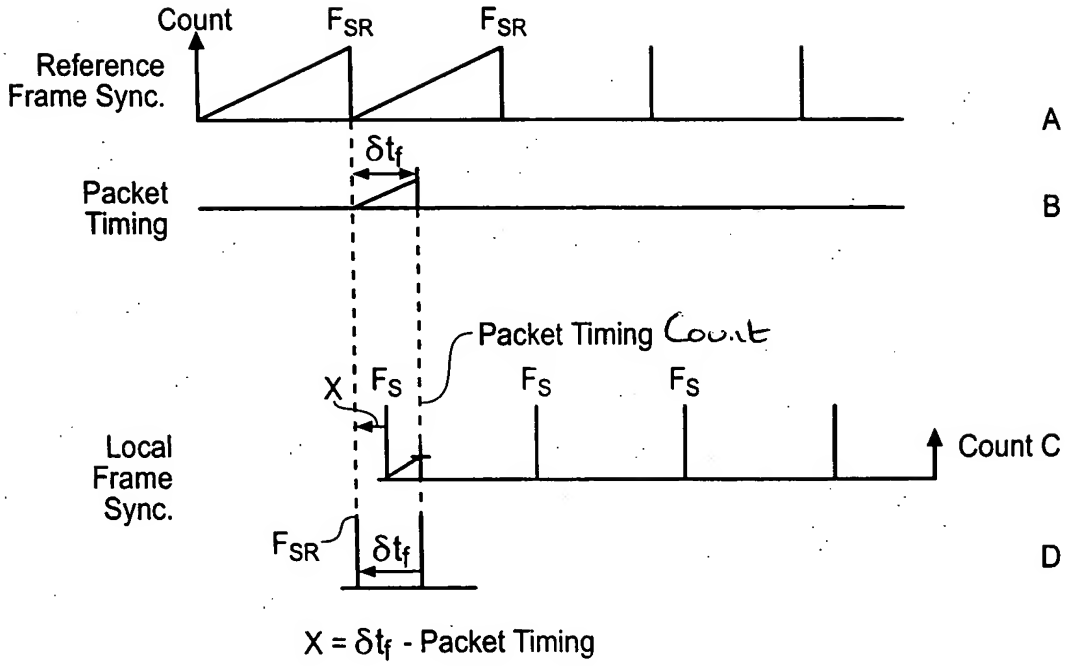

Count
F_{SR}
F_{SR}
Reference
Frame Sync.
A
δt_f
Packet
Timing
B
Packet Timing Count
X
F_S
F_S
F_S
Local
Frame
Sync.
Count C
F_{SR}
δt_f
D
X = δt_f - Packet Timing

Fig. 10

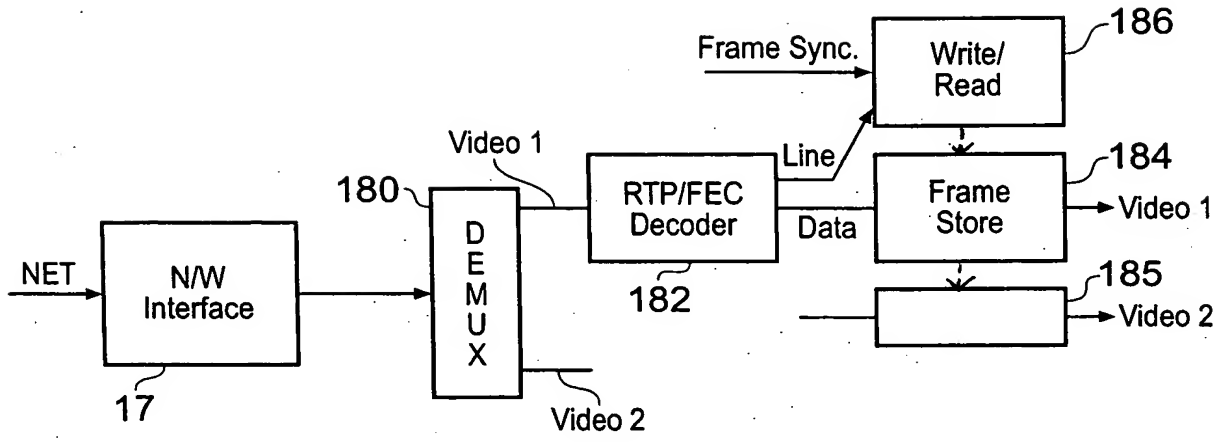

Frame Sync.
Write/
Read
186
Video 1
180
Line
184
RTP/FEC
Decoder
Frame
Store
Video 1
NET
N/W
Interface
DEMUX
Data
182
185
Video 2
17
Video 2

Fig. 12

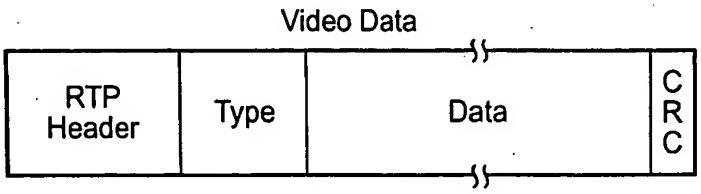

Video Data
RTP
Header
Type
Data
CRC

Fig. 13